RESEARCH ARTICLE OPEN ACCESS

# Traffic Light Controller Using Fpga

D.Bhavana[1], D.Ravi Tej[3], Priyanshi Jain[2], G.Mounika[2], R.Mohini[2] .Bhavana[2]
Asst.Professor, KLUniversity[1], Graduating students of KLUniversity[2] , Asst.Professor, SRK Institute of Technology

***Abstract***
The traffic light sequence works on the specific switching of Red, Green and Yellow lights in a particular way with stipulated time form. The normal function of traffic lights requires sophisticated control and coordination to ensure that traffic moves as smoothly and safely as possible and that pedestrians are protected when they cross the roads [1].This Traffic Light sequence is generated using a specific switching mechanism which will help to control a traffic light system on a road in a specified sequence. This paper focuses on the fact that the traffic lights can be varied in the day and night mode depending on the intensity of the traffic. It plays a vital role in supervising and running the metropolitan traffic and evade the possibilities of any unfortunate mishaps happening in and around the cities. It is a sequential machine to be scrutinized as per the requirements and programmed through a multistep development process. The methods that are used in this project are proposing the circuit, write a code, simulate, synthesis and implement on the hardware [8]. In this project, XILINX Software was chosen to devise a schematic using schematic edit, write a code using Verilog HDL (Hardware Description Language) text editor and implements the circuit on Programmable Logic Device [PLD].The system has been successfully tested and implemented in hardware using Nexys 2 Digilent FPGA.
**Keywords**: FPGA, Xilinx, Traffic Light Controller

## I. INTRODUCTION

**1.1: Need for Traffic Light Controller**
Traffic jamming is a critical predicament in many of the cities and towns all over the world [1]. Traffic congestion has been causing many setbacks and challenges in the major and most occupied cities all over the globe. To travel within the cities to the place of work or recreation has become a big problem to the commutates all along. Due to these problems people lose time, money and most importantly the energy resources will be exhausted due to the continual use in the automobiles. This traffic jam directly impacts the productivity of the workers, traders, suppliers and in all effecting the market and raising the prices of the commodities in a way. To solve these traffic related problems, we have to build new conveniences & infrastructure but at the same time make it smart. The only drawback of making new roads on facilities is that it makes the surroundings more congested, but then this will make a way to have new ways to ease the traffic. Perhaps all the countries are working to accommodate the traffic flow and advance transportation and reduce the demand of vehicle use.

We have to build new facilities and infrastructure making its use smarter for its efficient use. For this many ideas about the traffic light systems have come up in the recent past to simplify the complex problem of the traffic congestion. Mostly we see that the time allocation is fixed for east and west side, similarly for north and south direction in a traffic light controller at crossroads.

Traffic light controller (TLC) has been implemented using microcontroller FPGA, and ASIC design. FPGA has many advantages over microcontroller, some of these advantages are; the speed, number of input/output ports and performance which are all very important in TLC design, at the same time ASIC design is more expensive than FPGA[5].

## II. FPGA

Field Programmable Gate Arrays (FPGAs) are expansively used in quick prototyping and verification of conceptual design and also used in electronic systems where the mask-production of a custom IC becomes really expensive due to the small quantity [2]. The use of the FPGA's is increasing to avoid the high costs for a custom VLSI for a small quantity.

Many system designs that used to be built in custom silicon VLSI are now implemented in Field Programmable Gate Arrays [3].

**FPGA Design Flow**

A simplified version of design flow is given in the following block diagram

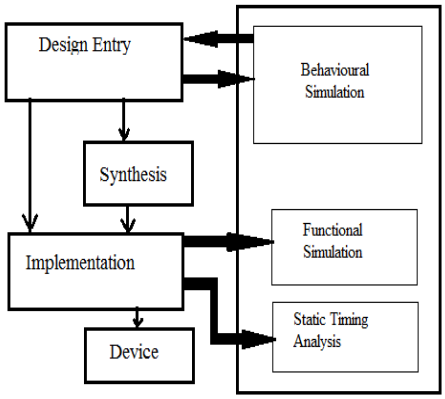


**Fig.1 Block diagram for FPGA simulation**

**Design Entry**

There are various techniques for design entry. Schematic based, Hardware Description Language and combination of both etc. Selection of a method depends on the design and designer. If the designer wants to deal more with Hardware, then Schematic entry is the good choice. When the design is complex or the designer thinks the design in an algorithmic way then HDL is the better choice. Language based entry is faster but lag in performance and density.

HDLs represent a level of abstraction that can separate the designers from the details of the hardware implementation. Schematic based entry gives designers much more visibility into the hardware. It is the good choice for those who are hardware adapted to. Another method but rarely used is state-machines. It is the better choice for the designers who think the design as a series of states. But the tools for state machine entry are limited. In this documentation we are going to deal with the HDL based design entry.

**Synthesis**

The process which translates VHDL or Verilog code into a device net list format .i.e. a complete circuit with logical elements (gates, flip flops, etc…) for the design.If the design contains more than one sub designs, ex. to implement a processor, we need a CPU as one design element and RAM as another and so on, then the synthesis process generates net list for each design element.

Synthesis process will check code syntax and analyse the hierarchy of the design which ensures that the design is optimized for the design

## III. Design of Traffic Light Controller

Traffic Light Controller can be designed by starting with certain assumptions. Initially Red signal is ON in North, East, West and South direction. Now when the Reset is made high the North traffic will be allowed to move and traffic in all the remaining directions are stopped. Later the traffic in all the other direction is allowed to move in the sequence. The advantage of this particular Traffic Light Controller program is that modification can be done easily as per the requirements i.e., suppose the traffic on main road and the side road can be controlled by changing the states accordingly, when the main road traffic is heavy when compared to the side road traffic[2]. In general Traffic light controller System consists of three lights (red, green and yellow) in each direction .The red light indicate Stop, green light indicate to allow the traffic and yellow light indicates the caution that the traffic is going to be stopped in few seconds.

The traffic light controller is a sequential circuit and is modelled as a finite state machine[6].

**Explanation of Traffic Light Controller**

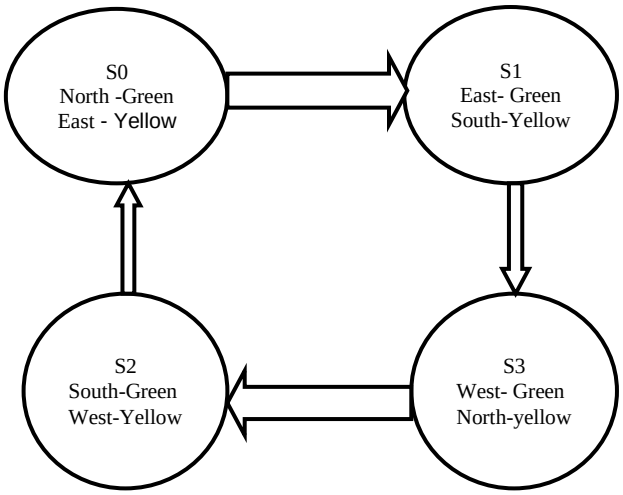


**Fig.2. State Diagram for traffic light controller**

There are four traffic light signals, in the below figure represented by R1, R2, R3 and R4 which are to be controlled. These four signals have same priority as they all are main roads.

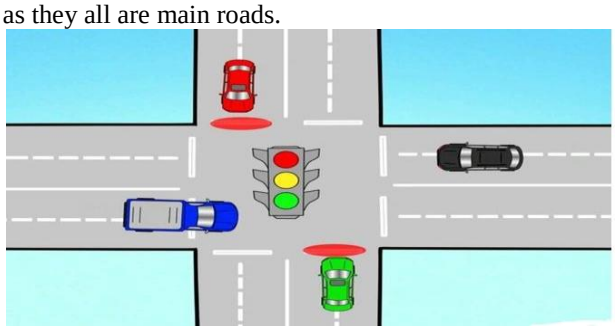

**Fig 3. Signals at Junction**

First of all the directions are red. When the reset mode is ON the signal of North direction is green, East direction is yellow remaining all the directions are Red. This state is particular assigned as S0.

Later the controller is switched to state S1 where the North direction is yellow, south direction is yellow and the remaining directions are red. Next by switching the State to S2 South direction is green, West direction is Yellow. Finally during S3 state green is on in the west direction and yellow in north direction, the remaining directions are Red.

These states are changed manually. The switching of states and reset button is controlled by the user. This is one of the most advantages in this project.

| Select lines | | DIRECTIONS | | | |
|---|---|---|---|---|---|
| $S_1$ | $S_0$ | NORTH | EAST | SOUTH | WEST |
| Initial | | RED | RED | RED | RED |
| 0 | 0 | GREEN | YELLOW (A) | RED | RED |
| 0 | 1 | RED | GREEN | YELLOW (b) | RED |
| 1 | 0 | RED | RED | GREEN | YELLOW(C) |
| 1 | 1 | YELLOW (d) | RED | RED | GREEN |

**Fig2.Tabular Column**

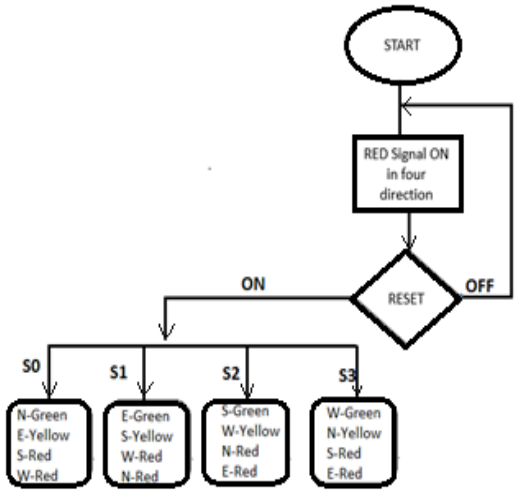


**Fig5. Flow chart for Simulation**

The flow chart can be applied to any number of road structures. In this paper, a four road structure is considered in which the four directions labeled with four labels namely North, South, East and West[4]

## IV. Simulation Results

### RTL Schematic

The figure below shows the RTL Schematic diagram of the Traffic Light Controller. Viewing a schematic allows you to see a technology level representation of your HDL optimized for specific device architecture, which may help to you discover the design issues early in design process[7].

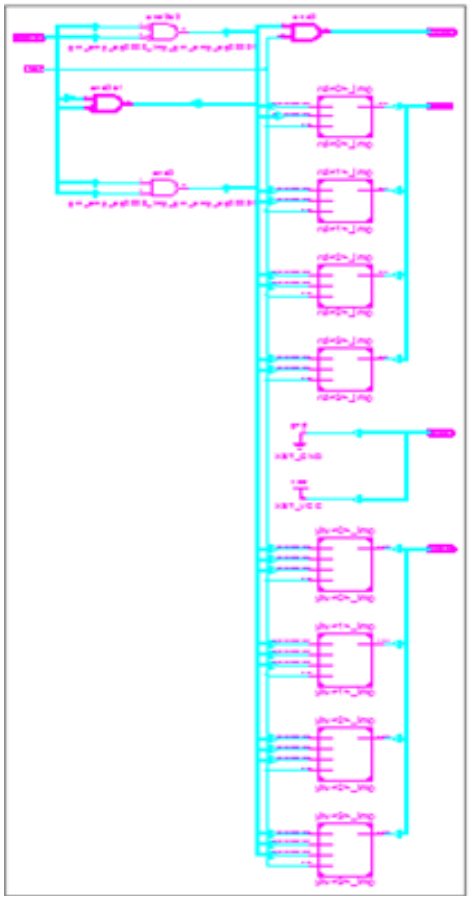

**Fig6. RTL Schematic**

### Wave Forms

The below figure shows the Wave form of the Traffic Light Controller when the test bench is applied to the source code.

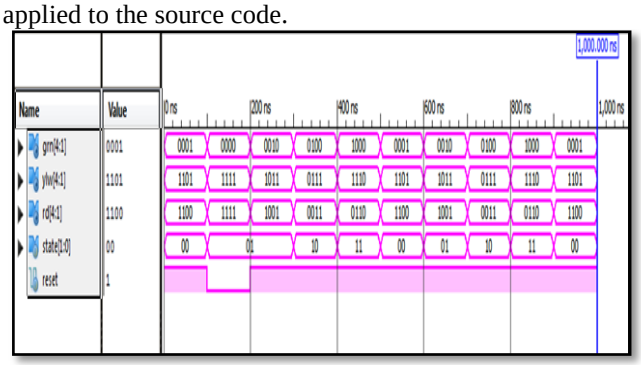


**Fig.7. Simulation results**

## V. Hardware Implementation

The Traffic Light Controller was designed using Verilog HDL and was implemented using FPGA. The output of the Traffic light controller is verified with NEXYS 2 FPGA.

Here we are using LED's & a 7-segment display to represent the outputs. Push buttons are used to opt for select lines.

The right most four LEDS corresponds to green lights on all four directions, left most LEDS stand for red lights on all four directions & 7- segment display signifies the yellow lights .

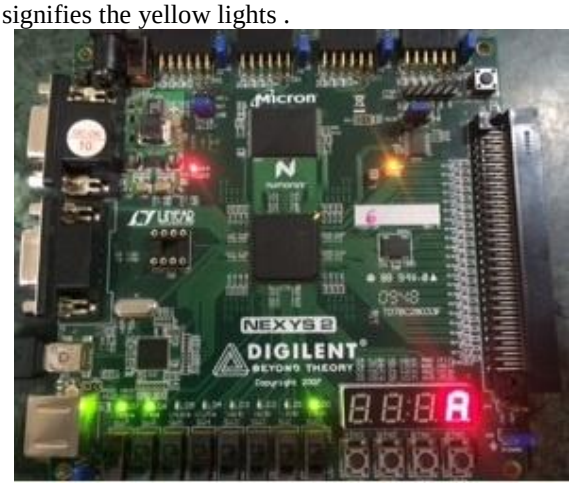


**Fig .8. Outputs on FPGA**

In the given sample output above, the select line is 00.The green light in NORTH direction is ON . The last two LEDS on left side representing RED lights on SOUTH &WEST directions respectively are also in ON state. The 7-segment display shows "A" which depicts Yellow which is ON in EAST direction.

## VI. Conclusion and Future Scope

The modern ways of four -way junction traffic light controller can improves the traffic condition up to a large extent. Advanced signaling controllers contribute to the improvement in the traffic condition; and also the prevention of the road accidents. This implementation of four junction traffic light controller can challenge any complexity in the traffic.

The future scope of this project is it can be directly applied in real time by employing more number of such circuits.

## References

[1] http://seminaprojects.org/t-traffic-signal-controller

[2] Mr. Prashant, Global journals.org/ GJRE_ Volume13/1-Designing-of-Automatic

[3] *"Design of FPGA Based Intelligence Traffic light Controller*", Sourav Nath, Suman Sau, Abhishek Roy ,2012 Conference on Radar, Communication & Computing, SKP College , Tiruvannamalai, TN, December .

[4] "*FPGA Implementation of an Advanced Traffic Light Controller using Verilog HDL*", Dilip, Y. Alekhya, P. Divya Bharathi ,Advanced Research in Computer Engineering & Technology; Volume 1, Issue 7,pp: 2278 – 1323,2012.

[5] **"***FPGA-Based Advanced Real Traffic Light Controller System Design***".** El-Medany, W.M. ; Univ. of Bahrain, Sakhir ; Hussain, M.R.DOI:10.1109/IDAACS.2007.4488383 Publisher:IEEE

[6] **"***Structural modeling of intelligent traffic light controller on fpga*" , surabhi s. gaopande, ashwini d. Bharade. Department of Electronics Engineering, Visvesvaraya National Institute of Technology, India. http://iraj.in/up_proc/pdf/101-141035116021-24.pdf

[7] .http://www.xilinx.com/itp/xilinx10/isehelp/ise_p_viewing_a_technology_schematic_xst.html

[8] http://www.3gwirelessjobs.com/resume/view/31206/planning-and-optimization-engineer-.html